3/24/03

Our Docket No.: 42390P7149

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Nizar, et al.	Examiner: **D. Tran**
Application No.: **09/420,887**	Art Group: **2186**
Filed: **October 19, 1999**	
For: **Method and Apparatus for Supporting SDRAM Memory on a Memory Channel**	

DECLARATION OF PRIOR INVENTION TO OVERCOME CITED PATENT OR PUBLICATION (37 C.F.R. § 1.131)

Commissioner for Patents
Washington, DC 20231-9999

Sir:

Purpose of Declaration

This declaration is to establish completion of the invention of this application in the United States at a date prior to February 26, 1999, that is the effective date of the prior art patent publication that was cited by the Examiner.

The person making this declaration is Puthiya K. Nizar, one of the two joint inventors. The second joint inventor, Khong S. Foo, is currently in Penag, Malayasia, and was not available to make this declaration in a timely manner.

Facts and Documentary Evidence

To establish the date of actual reduction to practice of the invention of this application, an Intel Invention Disclosure Document is submitted as evidence. From

this document it can be seen that the invention of this application was actually reduced to practice at least by a date that is prior to February 26, 1999, that is the effective date of the reference.

Time of Presentation of the Declaration

This declaration is submitted prior to final rejection.

Declaration

As a person signing below:

I hereby declare that all statements made herein of my own knowledge are true and that the statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature: Puthiya K Nizar

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INTEL INVENTION DISCLOSURE

INTEL CONFIDENTIAL

LEGAL ID# _____ Chipset/Graphics Comm /CEG/PCD DATE: A Date Prior to Feb. 26, 1999 P7149

It is important to provide accurate and detailed information on this form. The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to the Legal Department at JF3-147. If you have any questions, please call 264-0444 or 264-0998.

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(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

2. Title of Invention: A mechanism for supporting SDRAM memory on a Rambus Channel.
3. What technology/product/process (code name) does it relate to: Camino, Carmel MCHs, MTH, MRH-S
4. Stage of development (i.e. % complete) Camino TO ww39, Carmel TO ww51
5. (a) Has a description of your invention been, or will it shortly be, published outside Intel:
   NO: X YES: _____ DATE WAS OR WILL BE PUBLISHED: _____
   If YES, was the manuscript submitted for pre-publication approval? YES: _____ NO: _____

   (b) Has your invention been used/sold or planned to be used/sold by Intel or others?
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   (c) Does this invention relate to technology that is or will be covered by a SIG (special interest group)/standard/ or specification?
   NO: No YES: _____ Name of SIG/Standard/Specification: _____

   (d) If the invention is a semiconductor device, actual or anticipated date of tapeout? A Date Prior to
   (e) If the invention is software, actual or anticipated date of any beta tests. Feb. 26, 1999

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6. Was the invention conceived or constructed in collaboration with anyone other than an Intel blue badge employee or in performance of a project involving entities other than Intel, e.g. government, other companies, universities or consortia?
   NO: No YES: _____ Name of individual or entity: _____

PLEASE READ AND FOLLOW THE DIRECTIONS ON THE ATTACHED PAGE ON HOW TO WRITE A DESCRIPTION OF YOUR INVENTION

A Date Prior to

Please attach a page to this form, DATED AND SIGNED BY AT LEAST ONE PERSON WHO IS NOT A NAMED INVENTOR, to provide a description of the invention, and include the following information:

1. **Describe in detail how the invention works.**
2. **Describe advantage(s) of your invention over what is done now.**
3. **Include at least one figure illustrating the invention. If the invention relates to software, include a flowchart or pseudo-code representation of the algorithm.**
4. **Value of your invention to Intel (how will it be used?).**
5. **Identify the closest or most pertinent prior art that you are aware of.**
6. **Who is likely to want to use this invention or infringe the patent if one is obtained and how would infringement be detected?**

***HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM**

DATE: A Date Prior to Feb. 26, 1999 **SUPERVISOR:** _____

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID

A mechanism for supporting SDRAM memory on Rambus memory channel.

Abstract:

This invention describes a novel way of connecting SDRAM memory on a Rambus channel through a "Rambus to SDRAM" translator chip known as MTH (Memory Translator Hub). This translator chip interprets a new set of protocol on the physical Rambus channel and generates appropriate SDRAM commands to the SDRAM memory array. The control signals on the Rambus channel are used for sending SDRAM specific commands from the memory controller to the MTH. The protocol used between the memory controller (MCH) and MTH is different from RDRAM protocol. The data signals on the Rambus channel are used for data transfer between MCH and MTH. Multiple MTHs can be connected on the Rambus channel and each MTH can support multiple SDRAM rows. Also the MTH supports interleaved and non interleaved modes of operation.

General Purpose of Invention:

This invention allows us to support two different memory technologies (RDRAM and SDRAM) using a same physical Rambus channel.

Advantage of Invention over what is done now:

Since Rambus is new technology there is no prior art. This invention allows us to build cost effective and high performance SDRAM memory subsystem using high performance Rambus physical channel.

Essential Elements of Invention:

The Figure 1 below shows how SDRAM memory array is supported on a Rambus channel by using MTH chip. The MTH chips shown in figure 1 below, supports only two SDRAM rows per chip. The initial implementations of MTH supports up to four or six rows of SDRAM per MTH.

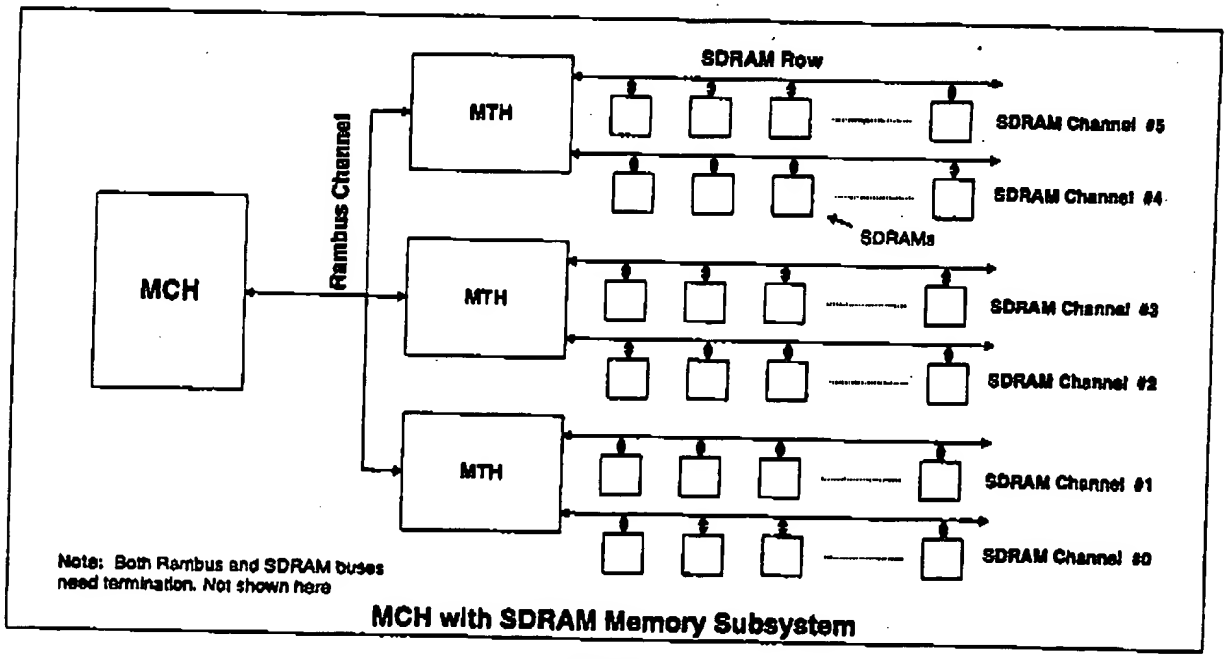

Figure 1

Operation Overview

The MTH receives commands from the memory controller through the Rambus channel. When it gets a command, it decodes it and drives appropriate signals on the SDRAM interface. For read commands it waits for the data to come back

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from the SDRAMs and then converts it to appropriate data packets to be sent to the memory controller. The MTH is aware of the CAS Latency (CL) for the SDRAMs and hence times them appropriately.

The MTH supports a modified version of RDRAM write protocol on Rambus. In order to support it, the MTH contains a write buffer to temporarily store the write data and control from MCH. It stores this data to SDRAM upon receiving a retire command (implied or explicit) from the MCH.

The MTH does the Current Calibration and Temperature Calibration of the Rambus channel upon receiving the commands from MCH.

The MTH contains registers for configuration and control. These registers are accessed through a three signal CMOS interface provided by Rambus channel.

A block diagram of internal logic blocks in MTH is shown below.

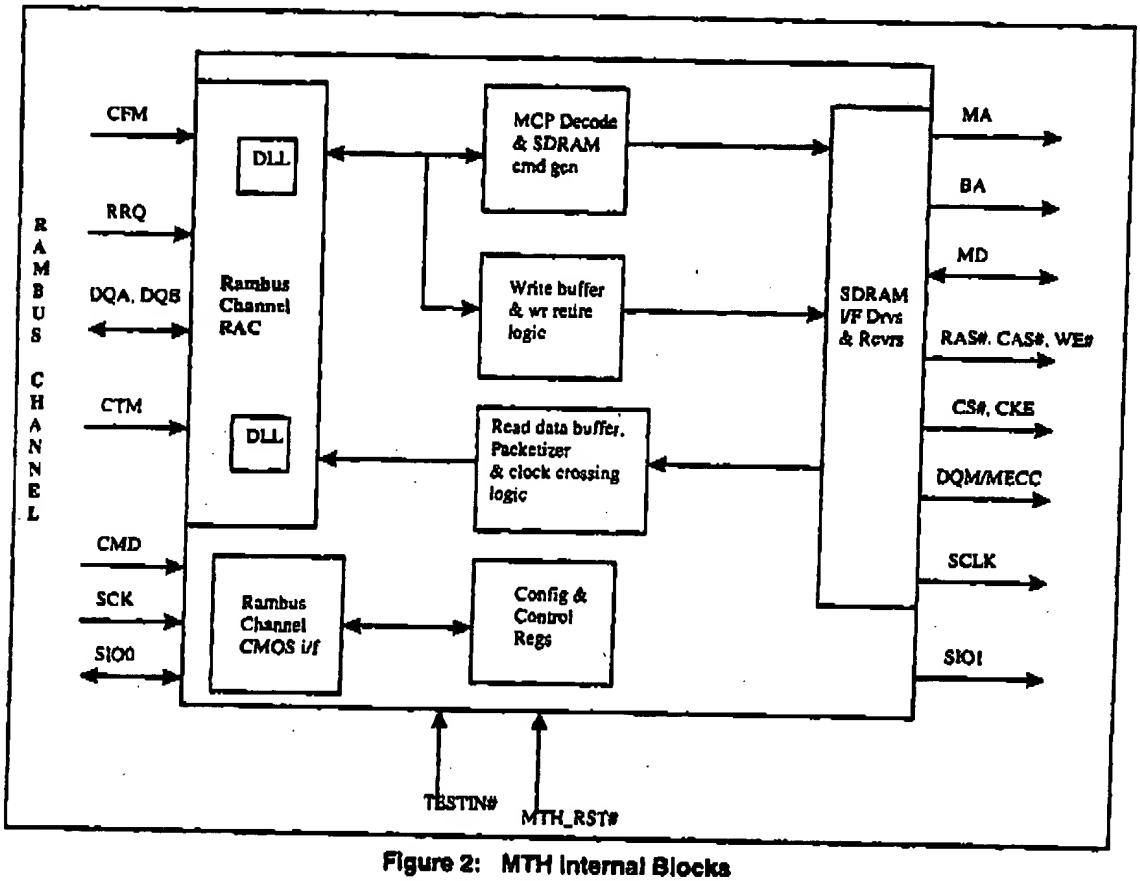

Figure 2: MTH Internal Blocks

Protocol Overview

For the Rambus Channel, there are two groups of high speed (RSL) control signals, a high speed (RSL) data and control bus, and a group of low speed CMOS control signals. The control signal groups are referred to as the Request Control (RQ) and data signals are referred to as DQA and DQB signals. The Request Control signals carry the Memory Control Packets (MCP) from MCH to MTH.

MCP Packet Format:

A command packet uses all 8 RSL request signals (RQ7: RQ0) on the channel to send a command from MCH to MTH. This command packet is known as MCP (Memory Control Packet). There are 32 bits in an MCP packet. The MCP packet is sent over the channel in two Rambus Channel clocks (RClks). (Note: The immediately following two Rclks must not be used for sending the next MCP). There are two bits (ST and SF) in the MCP packet to indicate the framing of a packet and to specify what kind of command packet it is. The encoding of ST and SF is shown below.

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Encoding of ST and SF:

ST	SF	Operation
0	0	No Framing
0	1	Frame an Activate Command
1	0	Frame a Read/Write Command
1	1	Frame an Extended Command

If the ST, SF is 0, 1 then the MCP packet specifies an Activate Command. The packet is:

MCP for Activate Command

	Cycle 0		Cycle 1	
RQ7	ST = 0	x	R[5]	x
RQ6	SF = 1	R[12]	R[4]	x
RQ5	r	R[11]	R[3]	x
RQ4	D[3]	R[10]	R[2]	B[0]
RQ3	D[2]	R[9]	R[1]	B[1]
RQ2	D[1]	R[8]	R[0]	DBM[3]
RQ1	D[0]	R[7]	r	DBM[2]
RQ0	r	R[6]	r	x

x = don't care

r = reserved. MCH must drive logic 0

D[3:0] = Specifies the targeted SDRAM row.

B[1:0] = Specifies the SDRAM bank address

R[12:0] = Specifies the SDRAM Row address

DBM[3:2] = Specifies which bit of the SDRAM row ID to mask out during decode in interleaved mode. These bits must be written to 0 in non-interleaved mode. DBM[3] is the mask bit for D[3] and DBM[2] is the mask bit for D[2]. When DBM[3] = 1, the MTH decodes D[3] as TRUE and only decodes D[2:0] to determine the row to direct the MCP to. When DBM[2] = 1, the MTH decodes D[2] as TRUE and only decodes D[3, 1:0] to determine the row to direct the MCP to.

Device Bit Mask

Two device ID mask bits are included in the MCP packets to allow more than one MTH to pre-charge or activate a page in its specified SDRAM row. These bits are used to enable masking out the upper two bits of the device ID (D[3], D[2]) during MTH SDRAM row decode. When the device bit mask is written to 1, the MTH comparison for the corresponding device bit is always TRUE, i.e. when DBM[3] = 1, the value of D[3] always matches in all MTHs on the bus regardless of the programming of the MTH ID MASK and only bits D[2:0] are used to select the targeted channel. Similarly, when DBM[2] = 1, the value of D[2] always matches in all MTHs on the bus regardless of the programming of the MTH ID MASK and only bits D[3, 1:0] are used to select the targeted channel. These bits (DBM[3:2]) are only valid in interleaved mode for pre-charge and activate commands. Setting these bits together with other commands or mode are not supported and are illegal.

The purpose of these bits is to allow the memory controller to treat two interleaved pages as a single, larger page. The larger page enables back-to-back interleaved reads and writes for page hit, miss and empty.

If the ST, SF is 1, 0 then the MCP packet specifies a Read or Write command. The packet is:

MCP for Read/Write Command

Cycle 0	Cycle 1

RQ7	ST = 1	x	C[5]	x
RQ6	SF = 0	x	C[4]	x
RQ5	R/W	C[10]	C[3]	x
RQ4	D[3]	AP	C[2]	B[0]
RQ3	D[2]	C[9]	C[1]	B[1]
RQ2	D[1]	C[8]	C[0]	r
RQ1	D[0]	C[7]	r	r
RQ0	r	C[6]	r	x

x = don't care

r = reserved. MCH must drive logic 0

D[3:0] = Specifies the targeted SDRAM row.

B[1:0] = Specifies the SDRAM bank address

C[10:0) = Specifies the SDRAM Column address

R/W = Specifies whether packet is for Read or Write. R/W = 0 = Read, R/W = 1 = Write

AP = Auto pre-charge AP = 0 = no auto pre-charge, AP = 1 = Auto pre-charge enabled

If the ST, SF is 1, 1 then the MCP packet specifies an Extended command. The packet is

MCP for Extended Commands (general)

	Cycle 0		Cycle 1	
RQ7	ST = 1	OP[8] / MA[7]	OP[5] / MB[7]	OP[2]
RQ6	SF = 1	OP[7] / MA[6]	OP[4] / MB[6]	OP[1]
RQ5	MASK	OP[6] / MA[5]	OP[3] / MB[5]	OP[0]
RQ4	D[3]	MA[4]	MB[4]	B[0]
RQ3	D[2]	MA[3]	MB[3]	B[1]
RQ2	D[1]	MA[2]	MB[2]	r
RQ1	D[0]	MA[1]	MB[1]	r
RQ0	BRD	MA[0]	MB[0]	x

x = don't care

r = reserved. MCH must drive logic 0

List of extended commands:

Nop

Retire w/ Mask

Pre-charge

Current Calibrate and Sample

Temperature Calibrate

Refresh

Self Refresh Entry

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Self Refresh Exit

Power-down Entry

Power-down Exit

Clock Stop

MCP for Retire w/ Mask

	Cycle 0		Cycle 1	
RQ7	ST = 1	MA[7]	MB[7]	x
RQ6	SF = 1	MA[6]	MB[6]	x
RQ5	MASK = 1	MA[5]	MB[5]	x
RQ4	D[3]	MA[4]	MB[4]	x
RQ3	D[2]	MA[3]	MB[3]	x
RQ2	D[1]	MA[2]	MB[2]	r
RQ1	D[0]	MA[1]	MB[1]	r
RQ0	0	MA[0]	MB[0]	x

x = don't care

r = reserved. MCH must drive logic 0

D[3:0] = Specifies the targeted SDRAM row.

MA[7:0] = Byte Masks for DQA bus (DQA is Rambus 8 bit data bus)

MB[7:0] = Byte Masks for DQB bus (DQB is Rambus 8 bit data bus).

MASK = Mask Field Valid, MASK = 1= MA[7:0] and MB7:0] specifies the mask field to be used when retiring the accompanying data

MCP for Extended Commands for Pre-charge

	Cycle 0		Cycle 1	
RQ7	ST = 1	OP[8]	OP[5]	OP[2]
RQ6	SF = 1	OP[7]	OP[4]	OP[1]
RQ5	0	OP[6]	OP[3]	OP[0]
RQ4	D[3]	V	x	B[0]
RQ3	D[2]	x	x	B[1]
RQ2	D[1]	x	x	DBM[3]
RQ1	D[0]	x	x	DBM[2]
RQ0	BRD	x	x	x

x = don't care

r = reserved. MCH must drive logic 0

D[3:0] = Specifies the targeted SDRAM row.

B[1:0] = Specifies the SDRAM bank address

BRD = Broadcast.

BRD = 1; This command is a broadcast command. All MTHs must execute this command to all of their SDRAM rows.

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BRD = 0; This command must be executed by the SDRAM row specified by D[3:0].

V = Valid value when pre-charge command is specified by OP8:OP0. When V is 1 during pre-charge, all banks are pre-charged.

DBM[3:2] = Specifies which bit of the SDRAM row ID to mask out during decode in interleaved mode. These bits must be written to 0 in non-interleaved mode. DBM[3] is the mask bit for D[3] and DBM[2] is the mask bit for D[2]. When DBM[3] = 1, the MTH decodes D[3] as TRUE and only decodes D[2:0] to determine the row to direct the MCP to. When DBM[2] = 1, the MTH decodes D[2] as TRUE and only decodes D[3, 1:0] to determine the row to direct the MCP to.

MCP for Extended Commands other than Retire w/ Mask and Pre-charge

	Cycle 0		Cycle 1	
RQ7	ST = 1	OP[8]	OP[5]	OP[2]
RQ6	SF = 1	OP[7]	OP[4]	OP[1]
RQ5	0	OP[6]	OP[3]	OP[0]
RQ4	D[3]	r	x	B[0]
RQ3	D[2]	x	x	B[1]
RQ2	D[1]	x	x	r
RQ1	D[0]	x	x	r
RQ0	BRD	x	x	x

x = don't care

r = reserved. MCH must drive logic 0

D[3:0] = Specifies the targeted SDRAM row.

B[1:0] = Specifies the SDRAM bank address

BRD = Broadcast. BRD = 1 = This command is a broadcast command. All MTHs must execute this command to all of their SDRAM rows.

BRD = 0 = This command must be executed by the SDRAM row specified by D[3:0].

OP[7:0] definition:

OP8	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Operation
0	0	0	0	0	0	0	0	0	No Op (No operation to be performed by MTH)
0	0	0	0	0	0	0	0	1	Pre-charge
0	0	0	0	0	0	0	1	0	Refresh
0	0	0	0	0	0	1	0	0	Self Refresh Entry
0	0	0	0	0	1	0	0	0	Self Refresh Exit
0	0	0	0	1	0	0	0	0	Power-down Entry
0	0	0	1	0	0	0	0	0	Power-down Exit
0	0	1	0	0	0	0	0	0	Clock Stop
0	1	0	0	0	0	0	0	0	Current Calibrate and Sample
1	0	0	0	0	0	0	0	0	Temperature Calibrate

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MCP packet for MTH synchronization

	Cycle 0 -	Cycle 0 +	Cycle 1 -	Cycle 1 +	Cycle 2 -	Cycle 2 +	Cycle 3 -	Cycle 3 +
RQ7	1	0	0	0	0	0	0	0
RQ6	1	0	0	0	0	0	0	0
RQ5	0	0	0	0	0	0	0	0
RQ4	0	0	0	0	0	0	0	0
RQ3	0	0	0	0	0	0	0	0
RQ2	0	0	0	0	0	0	0	0
RQ1	0	0	0	0	0	0	0	0
RQ0	1	0	0	0	0	0	0	0

Row/Column Address mapping to MA[12:0]

MA12 --- R12
MA11 --- R11 / C[10]
MA10 --- R10 / AP / V
MA9 --- R9 / C9
MA8 --- R8 / C8
MA7 --- R7 / C7
MA6 --- R6 / C6
MA5 --- R5 / C5
MA4 --- R4 / C4
MA3 --- R3 / C3
MA2 --- R2 / C2
MA1 --- R1 / C1
MA0 --- R0 / C0

SDRAM Command Truth Table

The following table shows the SDRAM command encoding for the respective MCP commands.

Function	SCLK n	SCLK n-1	CKE n	CKE n-1	CS#	RAS#	CAS#	WE#	A11	A10	BA[1:0]	A9-A0
NOP	R	R	H	x	L	H	H	H	x	x	x	x
Read	R	R	H	x	L	H	L	H	V	L	V	V
Read with auto-precharge	R	R	H	x	L	H	H	V	V	H	V	V
Write	R	R	H	x	L	H	L	L	V	L	V	V
Write with auto-precharge	R	R	H	x	L	H	L	L	V	H	V	V
Bank Activate	R	R	H	x	L	L	H	H	V	V	V	V
Precharge selected bank	R	R	H	x	L	L	H	L	V	L	V	x

Function	SCLK n	SCLK n-1	CKE n	CKE n-1	CS#	RAS#	CAS#	WE#	A11	A10	BA[1:0]	A9-A0
Precharge all banks	R	R	H	x	L	L	H	L	x	H	x	x
Refresh	R	R	H	H	L	L	L	H	x	x	x	x
Self Refresh Entry	R	R	H	L	L	L	L	H	x	x	x	x
Self Refresh Exit	R	R	L	H	H	x	x	x	x	x	x	x
Power-down Entry	R	R	H	L	H	x	x	x	x	x	x	x
Power-down Exit	R	R	L	H	H	x	x	x	x	x	x	x
Mode Register Set	R	R	H	x	L	L	L	L	L	L	V	V
Clock Stop	R	L	x	x	x	x	x	x	x	x	x	x

Legend:

x = Don't care, H = Logic high, L = Logic Low, R = clock running, V = Valid address

Current Calibration

Upon receiving a Current Calibrate and Sample command from MCH, the MTH must initiate current calibrate process of its RAC. For details on how to do the current calibration of RAC refer to Direct Rambus ASIC Cell Specification Version 0.7.

Temperature Calibration

Upon receiving the Temperature Calibrate command from MCH, the MTH must initiate temperature calibration process of its RAC. For details on how to do the temperature calibration of RAC refer to Direct Rambus ASIC Cell Specification Version 0.7.

SDRAM CBR Refresh

The MTH supports only CAS-before-RAS (CBR) refresh for active refresh. It sends the CBR command to an SDRAM row when it receives the appropriate MCP from MCH. Also, the MTH sends eight consecutive CBR commands (appropriately timed) to the specified SDRAM row upon receiving a Burst CBR serial command through the MOR register.

Self Refresh Entry and Exit

The MTH supports self refresh entry and exit MCP commands. These commands are used by the system to enter and exit the STR (Suspend to DRAM) state of the power management

Power-down Entry and Exit

The MTH supports Power-down Entry and Exit MCP commands.

Interleaved Operation

The MTH supports both interleaved and non-interleaved mode of operation.

Interleaved operation

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The interleaved mode of operation allows the memory controller to achieve up to 1.6Gbytes of SDRAM bandwidth by using pairs of MTHs and alternating command issues to MTHs. The Carmel MCH implements cache line based interleaving. In this scheme all "Odd Cache Line" accesses go to one MTH and all "Even Cache Line" accesses go to the other MTH.

The MTH allows the interleaving option by packetizing 16bytes of data from SDRAMs to send it over Rambus channel. This way only one packet (4 Rclks) is required on the Rambus channel to carry 16bytes of data from MTH to MCH. The disadvantage of interleaving is that it may add extra latency to memory reads due to the fact that the MTH has to waits for 16bytes of SDRAM data before it can sent the data packet to the MCH.

The interleaved mode is selected by programming bit 11 of MTR register. The default operation of MTH is non-interleaved.

Non-interleaved Operation

The MTH allows non-interleaved operation also. In the non-interleaved operation, the MTH sends the data packet to MCH in 8 bytes quantities. In this way the MTH can send the data as soon as it gets it from SDRAM. It does not have to wait for 16 bytes of data to accumulate and transferring 8 bytes of data reduces the latency. In this mode, the maximum data bandwidth is 800MB/s.

Registered DIMM support:

The MTH supports registered DIMMs with CAS latencies of 2 or 3. Bit [9] of the MTR register must be set to 1 to enable the registered DIMM operation. Also the appropriate tCAC value must be programmed.

SDRAM Command Issue Rules:

The MTH supports two timing modes for sending commands to SDRAM. These modes are known as 1n Rule and 2n Rule.

Single Cycle Command Rule

In this mode, the control signals, MA, RAS#, CAS# and WE# are driven to an SDRAM row in the same clock (SCLK) as the CS# for the row. This mode can be used for Registered DIMMs and SRIMMs/DIMMs with 9 or less loads in an SDRAM row. In this mode, the SDRAM bandwidth can be better managed by using the "unused" MCP slot between two read commands to SDRAM for doing SDRAM page management.

Two cycle Command Rule

In this mode, the control signals, MA, RAS#, CAS# and WE# are driven to an SDRAM row one clock (SCLK) earlier than the CS# for that row is driven. This mode is compatible with BX implementation and can be used for both DIMMs and SRIMMs that have more than 9 devices per row. Since the MCP slot between two consecutive SDRAM read commands cannot be used for anything, this mode is less efficient for SDRAM data bandwidth management. Typically the maximum data bandwidth will be less than 800MB/s.

Write Operation Policy

The MTH implements a modified version of RDRAM write protocol as described below. The MTH implements write buffer which will temporarily store the write data, address and control for up to two write commands from MCH. A 16byte data from the write buffer is sent to SDRAM when a retire command (explicit or implicit) is received by MTH. If the retire command specifies masked retire then the mask bits in the retire command must be used as DQM signals for writes to the SDRAM.

The rules for write operation are:

- The write data must be sent two SYNC clocks after the write MCP packet is sent. (i.e., the Write MCP in SYNC clock #0 and Write data in SYNC clock #2)
- For partial writes, the "Retire w/ Mask" MCP must be sent in the next SYNC clock after the write MCP is sent. The write data follows the Retire w/ Mask MCP packet.
- For full writes (i.e. all BE#s are asserted), no explicit Retire MCP is required. The MTH always retires the write data immediately after it gets the write data (see timing wave-forms for details).

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ECC Support

The MTH supports the ECC feature by passing the EEC code from the Rambus channel to SDRAM and vice versa. The MTH does not monitor the data for errors as it passes between the Rambus channel and the SDRAM array.

MTH Initialization:

The initialization of MTH is done by BIOS by programming the Initialization opcodes in SICM register of MCH. The initialization of MTH is done by BIOS by issuing SIO reset command and then programming the RIC field of the RAC initialization register

SDRAM Initialization

The SDRAM Initialization is done by BIOS by programming the MTOR register in MTH. This register is accessed through the Rambus CMOS interface signals SCK, SIO and CMD.

STR Support:

The MTH supports the STR power management state by maintaining the appropriate states on the SDRAM interface signals. The system puts MTH in STR state by executing the following sequences:

- Issue Self Refresh entry commands to all SDRAM rows
- Issue Stop Clock command to MTHs. (Upon receiving this command the MTH power downs the MTH RAC and then turns off the SDRAM PLL. This will turn off the SCLKs going to SDRAM rows.)
- Turn off the system clock generators.

The Vcc power to MTH must be maintained during STR. The following power sources must be kept alive to MTH during STR

- VCC25 ----- for MTH core
- VCC18 ----- for SCK, CMD, SIO and MTH_SIO interface
- VCC33 ----- for SDRAM interface

During STR exit, the BIOS does the initialization of MTH RAC after the Rambus channel clock is stable. The initialization includes current and temperature calibration of the RAC. The BIOS then issues synchronization packet to MTH. This will start the SDRAM clocks (SCLKs). The Self Refresh Exit can be issues after the MTHs are levelized.

System Clocking:

The MTH receives the differential Rambus clock from the DRCG clock generator chip in the system. From this clock the MTH generates two copies of SCLKs for SDRAM use. The SRIMMs that need more than two copies of SCLKs must use a PLL based clock buffer to generate the additional clock sources. A feedback input (SCLKFDBK) is provided on MTH to connect to an output from the clock buffer for phase alignment.

SDRAM Timing Parameters:

The MTH needs to be aware of only one SDRAM timing parameter to operate properly. This timing parameters is CAS Latency (CL). All other SDRAM timing parameters are taken care of by MCH. The MTH supports CAS latencies of 2 and 3.

Initialization

The following steps are performed by BIOS to initialize the memory subsystem after reset.

- Assign unique serial addresses to an MTH.
- Read all read-only registers and process the information.

- Update the necessary read-write registers.
- Repeat steps 1 to 3 for all MTHs.
- Levelize the Rambus Channel.

(For detailed information on MTH initialization refer to BIOS spec for Camino platforms)

Identify the closest or most pertinent prior art that you are aware of.

Not aware of this kind of power management for SDRAM memory arrays.

Who is likely to want to use this invention or infringe the patent if one is obtained and how would infringement be detected?

The other chip-set vendors may use this invention to achieve a low cost and high performance memory controller in their chip-sets.

Witness Date A Date Prior to Feb. 26, 1999

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